A New Redundancy Structure in Self-Aligned Contact Process

Background of the Invention

Field of the Invention

This invention relates to integrated circuits and electronic devices formed on a semiconductor substrate. Particularly, this invention relates to fuse link structures and methods of fabrication of fuse link structures that selectively implement redundant circuits with the integrated circuits.

Description of the Related Art

Often complex integrated circuits are formed on semiconductor substrates having redundant functional circuits. These redundant functional circuits are implemented to insure improved yields in the manufacture of the integrated circuits. To eliminate malfunctioning circuits and to substitute functioning redundant circuits for the malfunctioning circuits, fuse links are placed appropriately within the integrated circuits. An example of this is in memory integrated circuits such as dynamic random assess memory (DRAM) and static random access memory (SRAM). The memory array is formed with redundant rows and columns of memory cells connected to the row and column address decoders. Prior to final assembly of the memory integrated circuit into a functioning package, each integrated circuit chip or memory chip is tested for functionality. Those columns and rows of the memory array having

nonfunctioning memory cells are eliminated from the memory array and the redundant memory rows and columns are implemented within the array to replace the malfunctioning columns and rows.

To perform the removal of the malfunctioning circuits and to implement the redundant circuit, destructible fuse links are formed at appropriate connective locations between operating functions of the integrated circuits, the redundant circuit functions, and the malfunctioning circuits. The fuse links are selectively destroyed to open the connection of the fuse link.

Conventionally, the fuse link is a layer conductive material such as a metal, a heavily doped polycrystalline silicon, or a layer of heavily doped polycrystalline silicon covered with a layer of a metal alloyed with the heavily doped polycrystalline silicon. The layer of conductive material is covered with a transparent insulative layer to protect the conductive material from contamination from the external environment.

If the fuse is to be destroyed, the fuse is subjected to excessive current or to an intensive laser light to sufficiently heat the layer of conductive material to destroy it. Currently, the conventional method of destruction is the use of an intense laser light. This requires the covering insulative layer be sufficiently transparent and sufficiently thin to allow the laser light to penetrate directly to the layer of conductive material.

U.S. Patent 5,729,041 (Yoo et al.) describes a structure and method of forming a fuse and fuse window having a protective layer formed over them. The protective layer is highly transmissive to intense laser light while it is protective of the fuse and the surrounding insulating layers.

U.S. Patent 4,651,409 (Ellsworth et al.) describes a fuse programmable read only memory (PROM). The fuse programmable PROM has a merged vertical fuse/bipolar transistor.

U.S. Patent 5,754,089 (Chen et al.) describes a fuse structure in which a metallic frame is inserted between the interlayer dielectric insulation layers. The metallic frame is used as a mask to form the fuse window to simplify alignment and to minimize problems due to insulation residue on the surface of the fuse window layer.

U.S. Patent 5,567,643 (Lee et al.) describes a method for creating a guard ring around a fuse link. The guard ring prevents contaminants from diffusing through a window opening above a fuse link to adjacent semiconductor devises. The guard ring is an annular metal ring that penetrates two or more insulating layers and contacts to the semiconductor substrate.

Summary of the Invention

An object of this invention is to form a fuse link to implement redundant circuits within an integrated circuit.

Another object of this invention is to create a fuse link where an insulating layer over a conductive layer of the fuse link is sufficiently thin and sufficiently transparent to allow destruction of the conductive layer by an intense laser light.

To accomplish these and other objects, a redundancy structure for implementation of redundant circuits within an integrated circuit placed on a semiconductor substrate includes a fusible link. The fusible link is formed of a layer of a conductive material deposited upon an insulating layer of the semiconductor substrate connected between the redundant circuits and other circuits present on the integrated circuit. The insulating layer is generally a layer of field oxide placed on the surface of the semiconductor substrate. The layer of conductive material is either formed of a metal such as Aluminum (Al) or Tungsten (W), a heavily doped polycrystalline silicon, or an alloy of a metal such as Tungsten (W) and a heavily doped polycrystalline silicon.

A hard mask layer is placed upon the layer of conductive material during transistor processing to protect the layer of conductive material during formation of self-aligned sources and drains of transistors of the integrated circuit. The hard mask layer is removed from the layer of conductive layer for deposition of

interlayer dielectric layers on the semiconductor substrate to improve a fuse destruction to implement the redundant circuits.

An opening is formed in the interlayer dielectric layers to thin the interlayer dielectric layers to allow exposure of the layer of conductive material to facilitate destruction of the layer of conductive material.

The redundancy structure of this invention allows the redundant columns or rows of a DRAM array to be implemented and connected to the row address and column address decoders of the DRAM array to improve the yield of the DRAM array.

The hard mask layer is generally a single layer of silicon nitride or two layers composed of silicon dioxide and the second layer is silicon nitride. If the hard mask layer is a single layer of silicon nitride, it has of from approximately 1500Å to approximately 3000Å. However, if the hard mask layer is the two layer, the first layer of silicon dioxide has a thickness of from approximately 100Å to approximately 1000Å and the second layer of silicon nitride has a thickness of from approximately 1000Å to approximately 3000Å.

The opening in the interlayer dielectric above the layer of conductive material has a bottom portion that extends to between approximately 4000Å and approximately 10,000Å above the layer of conductive material. The interlayer

dielectric is a layering of an undoped oxide and a borophososilicate glass and is formed such that the bottom portion of the opening in the interlayer dielectric has sufficient transparency to allow destruction of the layer of conductive material.

The hard mask layer is too thick and is thus removed to allow destruction of the layer of conductive material.

Brief Description of the Drawings

Figs. 1a - 1l shows a cross-section of a semiconductor substrate as it is processed to form transistors of an integrated circuit and a fuse link used to implement the redundant circuit of the prior art.

Fig. 2 is a process flow diagram showing the steps to fabricate the transistors of the integrated circuit and the fuse link used to implement the redundant circuit of the prior art.

Figs. 3a-3c show a cross-section of a semiconductor as it is processed to form transistors of an integrated circuit and a fuse link used to implement the redundant circuit of this invention.

Fig. 4 is a process flow diagram showing the steps to fabricate the transistors of the integrated circuit and the fuse link used to implement the redundant circuit of this invention.

Detailed Description of the Invention

Refer to Figs. 1a-1l and Fig. 2 for a discussion of the conventional formation of a fuse link during the creation of the electronic components and transistors of an integrated circuit of the prior art. Fig. 1a shows the defining **100** of the active region **15** and the well region **20**. An insulating material **10** such as a field oxide is formed on the surface of the semiconductor substrate **5**. The insulating material is created with opening for the active region **15** and the well region **20**. The well region **20** is then doped with a material having a conductivity opposite that of the semiconductor substrate **5**.

Fig. 1b shows the growing **105** of a second insulating layer **25** that forms the gate oxide over the active region **15** and the well region **20**. The gate oxide conventionally has a thickness of from approximately 30Å to approximately 200Å. In Fig. 1c a layer of heavily doped polycrystalline silicon **30** is deposited **110** on the second insulating layer **25** above the active region **15** and the well region **20** to form the gates **40** of the transistors of the integrated circuits. Simultaneously, the layer **40** of the heavily doped polycrystalline silicon is deposited on the field oxide **10** to form the conductive layer **45** of the fuse link. The layer of heavily doped polycrystalline silicon has a thickness of from approximately 1500Å to approximately 3000Å. A metal **35** such as tungsten is then deposited on and alloyed with the layer **30** of the heavily doped

polycrystalline silicon to complete the deposition **110** of the gates **40**, the active region **15**, and the well region **20**. Simultaneously, again, the metal **35** is deposited on and alloyed with the layer **30** of heavily doped polycrystalline silicon to complete the formation of the conductive layer **45** of the fuse link. The alloyed tungsten silicide (WSi2) has a thickness of from approximately 300Å to approximately 1500Å.

Fig. 1d illustrates the deposition **115** of a hard mask **50** on the gates **40** of the transistors and the conductive layer **45** of the fuse link. The hard mask **50** is conventionally a silicon nitride (Si_xN_y) deposited to a thickness of from approximately 1500Å to approximately 3000 Å. Alternately, the hard mask **50** is a first layer of silicon dioxide (SiO_2) having a thickness of from approximately 100Å to approximately 1000Å with a second layer of silicon nitride (Si_xN_y) having a thickness of from approximately 1000Å to approximately 3000Å.

A photoresist material **55** is deposited **120** on the hard mask **55** as shown in Fig. 1e. The photoresist material has openings to expose the hard mask layer **50** in all areas of the semiconductor substrate except those areas that are the gates **40** of the transistors and the conductive layers **45** of the fuse link. The hard mask layer **50**, the alloyed metal silicon layer **35**, and the heavily doped polycrystalline silicon layer **30** are etched **125** leaving the gates **40** of the transistors and the conductive material **45** of the fuse link as shown in Fig. 1f.

The lightly doped drains and sources **60** of the transistors to be formed in the active region **15** and the well region **20** are implanted **130** as shown in Fig. 1g. The gates **40** are annealed **135** and the spacers **65** are formed as sidewalls for the gates **40** of the transistors and the conductive layer **45** of the fuse link as shown in Fig. 1h.

The surface of the semiconductor substrate is covered **140** with a photoresist having openings exposing the areas that are to be the sources and drains **70** of the transistors. A first heavy doping material is implanted in the active region **15** and a second heavy doping material of an opposite material is implanted in the well region **20** to form the sources and drains **70** of the transistors as shown in Fig. 1i. Fig. 1i illustrates a hard mask removal photoresist **75** deposited on the surface of the semiconductor substrate. The hard mask removal photoresist exposes **145** the hard mask layer **50** of the gates **40**, while covering the hard mask layer **50** on the conductive layer **45** of the fuse link. The hard mask layer **50** of the gates **40** is removed **150** with an etchant process while the hard mask layer **50** of the conductive layer **45** of the fuse link remains intact.

At least one layer of an insulating material such as an undoped silicon dioxide with a borophososilicate glass (BPTEOS) is deposited **155** on the surface of the semiconductor substrate to form the interlayer dielectric (IMD) as shown in Fig. 1k. As Fig. 1l illustrates, openings **85** and **90** are defined **160** and

etched **165** to form the self-aligned contacts (SAC) for the sources and drains **70** and the gates **40** of the transistors. At this same time, the opening **95** is defined **160** and etched **165** to create a window **95** in the interlayer dielectric **80**. The window **95** exposes the hard mask layer **50** above the conductive layer **45** of the fuse link.

The openings **85** and **90** allow the connection of the gates **40**, the drains and sources **70** to be interconnected **170** in the back end of the line process to form the integrated circuits.

The self-aligned contact process forces the hard mask layer **50** to be thicker than is desired for sealing the conductive layer **45** of the fuse link from the external atmosphere. The additional thickness of the hard mask layer is to provide better "etch stop" during processing of the transistors. However, the additional thickness causes a complex fuse structure that has a low "repair rate" when the fuses are destroyed with an intense laser light.

To mitigate the problems of the thickness of the hard mask of the conventional forming of the fuse link and the transistors of the integrated circuits, the hard mask layer **50** covering the conductive layer **45** of the fuse link is removed. The interlayer dielectric **80** is formed over the conductive layer **45** of the fuse link. The window **95** is formed to create the necessary opening in the interlayer dielectric.

Refer to Figs. 3a-3c and Fig. 4 for a complete discussion of the formation of the fuse link of this invention. The conductive layer **45** of the fuse link and the transistors of the integrated circuit are formed as described above for Fig. 2 step **100** though step **140**. At step **445**, a photoresist **75** is deposited on the surface of semiconductor substrate **5**. Openings in the resist above the hard mask layer **50** of the conductive layer **45** and the gates **40** of the transistors permit the hard mask layer to be etched **150** to remove the hard mask layer **50** above the conductive layer **45** of the fuse link and the gates **40** of the transistors. The interlayer dielectric layer **80** is deposited **155** on the surface of the semiconductor substrate **5**. The openings **90** and **95** are defined **160** with a photoresist and etched **165** to form the self-aligned contact areas of the transistors. The metalization is formed during the back end of the line process **170** to interconnect the transistors to form the integrated circuits.

The opening **85** is defined **160** with a photoresist and etched **165** to form the window above the conductive layer **45**. The interlayer dielectric **80** is etched until a bottom portion **97** of the opening **85** approaches to within 4000Å and approximately 10,000Å of the conductive layer **45** of the fuse link. The thickness of the interlayer dielectric **80** at the bottom portion **97** of the window **95** must be sufficiently transparent to allow transmission of laser light to permit destruction of conductive layer **45** of the fuse link. At the same time, the thickness of the interlayer dielectric **80** at the bottom portion **97** of the window **95** must be

sufficiently thick to prevent contamination of the conductive layer **45** of the fuse link from atmospheric exposure.

While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

The invention claimed is: